

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231 www.uspto.gov

APPLICATION NO. FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO. 09/711,504 11/14/2000 Tsuyoshi Katoh 325739/99 8052

21254

7590

10/21/2002

MCGINN & GIBB, PLLC 8321 OLD COURTHOUSE ROAD SUITE 200 VIENNA, VA 22182-3817

EXAMINER SEFER, AHMED N

ART UNIT PAPER NUMBER

2814

DATE MAILED: 10/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
, Office Action Summary	09/711,504	KATOH ET AL.
	Examiner	Art Unit
	A. Sefer	2826
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply		
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status		
1) Responsive to communication(s) filed on <u>08 July 2002</u> .		
2a) This action is FINAL . 2b)⊠ This action is non-final.		
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.		
Disposition of Claims	P P	
4) Claim(s) 1-7 and 13-23 is/are pending in the application.		
 4a) Of the above claim(s) is/are withdrawn from consideration. 5)⊠ Claim(s) <u>13 and 14</u> is/are allowed. 		
6)⊠ Claim(s) <u>1-3,6,7 and 15-23</u> is/are rejected.		
7) Claim(s) <u>4 and 5</u> is/are objected to.		
8) Claim(s) are subject to restriction and/or election requirement. Application Papers		
9)☐ The specification is objected to by the Examiner.		
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.		
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).		
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.		
If approved, corrected drawings are required in reply to this Office action.		
12)☐ The oath or declaration is objected to by the Examiner.		
Priority under 35 U.S.C. §§ 119 and 120		
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).		
a) ☐ All b) ☐ Some * c) ☐ None of:		
1. Certified copies of the priority documents have been received.		
2. Certified copies of the priority documents have been received in Application No		
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 		
14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).		
 a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121. 		
Attachment(s)		
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7.		(PTO-413) Paper No(s) atent Application (PTO-152)
S. Patent and Trademark Office		

Art Unit: 2826

DETAILED ACTION

Response to Amendment

1. The amendment filed on 7/8/02 has been entered. Claims 8-12 have been cancelled and new claims 13-23 have been added.

Applicant is advised that should claims 1 and 7 be found allowable, claim 16 will be objected to and should claims 1 and 6 be found allowable, claim 15 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 3. Claims 1, 7 and 16 rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. US Patent No. 5,818,070.

Yamazaki et al. disclose (see fig. 2, col. 2, lines 46-57 and col. 7, lines 6-11) a

Application/Control Number: 09/711,504 Page 3

Art Unit: 2826

thin film transistor including a back channel electrode 114/115, wherein a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode 104/105 through a contact-hole (not shown) provided in a portion of a semiconductor layer having an ohmic contact layer on the side thereof, which is in contact with source and drain electrodes (as in claim 7) forming said thin film transistor.

- 4. Claims 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen US Patent No. 5,965,916.
- Chen discloses in figs. 3-5 a transparent substrate 1; a gate electrode 10 on a surface of said substrate; a gate insulating film 11 formed on said gate electrode; a semiconductor layer 12 formed on said gate insulating film; an ohmic contact layer 13 comprising a first side and a second side and a channel therebetween (as in claim 18) formed on said semiconductor layer.

As to claim 19, Chen discloses a source electrode 16 on said first side of said ohmic contact layer; and a drain electrode 16 on said second side of said ohmic contact layer.

5. Claims 17-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamazaki et al. (JP 2000-166093).

Yamazaki et al disclose in fig. 1 a transparent substrate100; a gate electrode 102a on a surface of said substrate; a gate insulating film 103 formed on said gate electrode; a semiconductor layer formed on said gate insulating film; an ohmic contact

Art Unit: 2826

layer 104 comprising a first side and a second side and a channel therebetween 112 (as in claim 18) formed on said semiconductor layer.

As to claim 19, Yamazaki et al disclose a source electrode 109 on said first side of said ohmic contact layer; and a drain electrode 111 on said second side of said ohmic contact layer.

As to claims 20 and 21, Yamazaki et al disclose a passivation film 106 comprising silicon nitride (as in claim 21) formed on said gate electrode; and a back channel electrode 107a formed on said passivation film.

6. Claims 17-21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. US Patent No. 5,818,070.

Yamazaki et al disclose in fig. 2 a transparent substrate101; a gate electrode 104 on a surface of said substrate; a gate insulating film 106 formed on said gate electrode; a semiconductor layer 108 formed on said gate insulating film; an ohmic contact layer 104 comprising a first side and a second side and a channel therebetween 133, 134 (as in claim 18) formed on said semiconductor layer.

As to claim 19, Yamazaki et al disclose a source electrode 139 on said first side of said ohmic contact layer; and a drain electrode 140 on said second side of said ohmic contact layer.

As to claims 20 and 21, Yamazaki et al disclose a passivation film 110 comprising silicon nitride (as in claim 21) formed on said gate electrode; and a back channel electrode 114a formed on said passivation film.

Application/Control Number: 09/711,504 Page 5

Art Unit: 2826

As to claim 23, Yamazaki et al disclose a back channel electrode electrically connected to a gate electrode through a gate contact hole.

7. Claims 17-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakurai et al. (JP 10-290012).

Sakurai et al disclose in figs. 4 and 9 a transparent substrate101; a gate electrode 1/102 on a surface of said substrate; a gate insulating film 103 formed on said gate electrode; a semiconductor layer 104 formed on said gate insulating film; an ohmic contact layer 104' comprising a first side and a second side and a channel therebetween (as in claim 18) formed on said semiconductor layer.

As to claim 19, Sakurai et al disclose a source electrode 5 on said first side of said ohmic contact layer; and a drain electrode 3 on said second side of said ohmic contact layer.

As to claims 20-22, Sakurai et al disclose a passivation film 105' comprising silicon nitride (as in claim 21) formed on said gate electrode; and a back channel electrode 9 comprising ITO (as in claim 22) formed on said passivation film.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Art Unit: 2826

9. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al US Patent No. 5,818,070 in view of Sakura et al. (10-290012).

Yamazaki et al disclose all the claimed subject matter but fail to disclose a back channel electrode formed of the same material as a material of a pixel electrode connected to one of source and drain electrodes.

Sakura et al disclose a back channel electrode 9 formed of the same material as a material of a pixel electrode 8 or a transparent electrode (as in claim 3) connected to one of source and drain electrodes.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Sakura et al with the device of Yamazaki et al, since that would reduce patterning process and increase yield.

10. Claims 15 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. US Patent No. 5,818,070 in view of Miyajima (JP 6-230425).

Yamazaki et al. disclose (see fig. 2, col. 2, lines 46-57 and col. 7, lines 6-11) a thin film transistor including a back channel electrode 114/115, wherein a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode 104/105 through a contact-hole (not shown) provided in a portion of a semiconductor layer forming said thin film transistor, but fail to disclose a semiconductor layer having equal width as a source and drain electrodes.

Art Unit: 2826

Page 7

Miyajima discloses in figs. 1-8 a semiconductor layer 15 patterned to have a width equal to a source and drain electrodes 25, 23 of a TFT provided between said source and drain electrodes and gate insulating film 14.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Miyajima 's teachings with the device of Yamazaki et al, since that would prevent shorting and improve yield as taught by Miyajima.

Allowable Subject Matter

- 11. Claims 13 and 14 are allowed.
- 12. Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS October 8, 2002 NATHAN J. FLYNN SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800